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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,019	01/16/2004	Lih-Chung Kuo	IBMS.070PA(0511)	8505
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DAVID W. LYNCH CHAMBLISS, BAHNER & STOPHEL 1000 TALLAN SQUARE-S TWO UNION SQUARE CHATTANOOGA, TN 37402			EXAMINER FRANKLIN, RICHARD B	
			ART UNIT 2181	PAPER NUMBER
			MAIL DATE 06/08/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/760,019

Applicant(s)

KUO ET AL.

Examiner

Richard Franklin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 9-18, 22 and 24-29 is/are rejected.
- 7) ☒ Claim(s) 6, 7, 19-21 and 23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1 – 29 are pending.

***Reopening of Prosecution After Appeal Brief***

2. In view of the Appeal Brief filed on 10 January 2007, PROSECUTION IS  
HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 10 recites the limitation "an external interface" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the "external interface" recited earlier in the claim or a new "external interface."

The Examiner has interpreted the limitation as referring to the "external interface" previously recited in the claim.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 – 4, 11 – 15, 22, and 27 – 29 rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,948,081 (hereinafter Foster) in view of US Patent Application Publication No. 2005/0273528 (hereinafter Adams) and further in view of US Patent Application Publication No. 2003/0079059 (hereinafter Tsai).

As per claims 1, 11, 27, and 29, Foster teaches gathering writes in a buffer (Foster; Figure 2 Item 46) before transmitting a burst of writes over an external bus (Foster; Col 7 Lines 37 – 41); monitoring the buffer to determine a number of writes in the buffer and whether the number of writes in the buffer exceed a predetermined threshold (Foster; Col 7 Lines 30 – 35).

Foster does not teach identifying an error condition when the number of writes in the buffer exceed the predetermined threshold and providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

However, Adams teaches that if a buffer overrun has occurred, an error condition is forced on the system (Adams; Figure 10 Items 174 and 176, Paragraphs [0025] and [0072]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Foster to include the error condition because doing so allows for avoidance of further system errors (Adams; Paragraph 0073)).

Foster in combination with Adams does not teach providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

However, Tsai teaches providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold (Tsai; Paragraph [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Foster in combination with Adams to include the rate controlling because doing so allows for data to be transferred correctly (Tsai; Paragraph [0005]).

As per claim 2, Tsai also teaches slowing writes to the buffer (Tsai; Paragraph [0005]).

As per claim 3, Foster also teaches wherein the gathering writes in a buffer before transmitting a burst of writes over an external bus further comprises transmitting a burst of writes over a bus (Foster; Col 7 Lines 57 – 59).

As per claims 4 and 15, Adams also teaches initiating error recovery in response to the overflow error (Adams; Paragraph [0025]).

As per claim 12, Foster also teaches an external interface coupled to the buffer, the external interface linking the buffer to the external bus (Foster; Figure 2 Items 36 and 40).

As per claim 13, Foster in combination with the Examiners taking of Official Notice and Tsai also obviously teach wherein the external bus comprises a PCI-X bus

because such busses are well known in the art as a high speed bus used in computer systems to connect peripheral devices.

As per claim 14, Foster also teaches a processor interface coupled to the buffer, the processor interface linking the buffer to a processor bus (Foster; Figure 2 Item 34).

As per claim 22, Adams teaches wherein the buffer monitor monitors the buffer, the external bus, and the processor bus for error conditions (Adams; Paragraph [0065])

5. Claims 5, 8, 16 – 18, and 24 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,948,081 (hereinafter Foster) in view of US Patent Application Publication No. 2005/0273528 (hereinafter Adams) further in view of US Patent Application Publication No. 2003/0079059 (hereinafter Tsai) and further in view of US Patent Application Publication No. 2005/0138471 (hereinafter Okbay).

As per claims 5 and 16, Foster in combination with Adams and Tsai teach the method and system as described per claims 1 and 11 (See rejection of claims 1 and 11 above).

Foster in combination with Adams and Tsai does not teach providing an arbitration signal for controlling access to the external bus in response to the comparison of the writes in the buffer to the predetermined threshold.

However, Okbay teaches arbitrating for an external memory bus when a buffer threshold is reached (Okbay; Paragraph [0038] Lines 5 – 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Foster in combination with Adams and Tsai to include the bus arbitration because doing so allows for increased bus throughput.

As per claims 8 and 25, Foster in combination with Adams and Tsai teach the method and system as described per claims 1 and 11 (See rejection of claims 1 and 11 above).

Foster in combination with Adams and Tsai does not teach clearing the buffer when the writes in the buffer exceed the predetermined threshold.

However, Okbay teaches flushing the buffer in response to the buffer exceeding the predetermined threshold (Okbay; Figure 5 Item 540, Paragraph [0047] Lines 2 – 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Foster in combination with Adams and Tsai to include the buffer flushing because doing so allows for more data to be inserted into the buffer without overwriting old data still in the buffer.

As per claim 17, Foster in combination with Adams and Tsai teach the system as described per claim 11 (See rejection of claim 11 above).

Foster in combination with Adams and Tsai does not teach wherein the buffer monitor comprises bus arbitration and control logic for controlling the movement of data onto the external bus.



However, Okbay teaches wherein the buffer controller (Okbay; Figure 2 Item 240) with arbitration control and data movement control (Okbay; Paragraph [0038] Lines 1 – 10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Foster in combination with Adams and Tsai to include the bus arbitration and data movement logic because doing so allows for the buffer controller to make room for new data to be added to the buffer.

As per claim 18, Okbay also teaches wherein the buffer bursts onto the external bus (Okbay; Figure 5 Item 540, Paragraph [0047] Lines 6 – 8).

As per claim 24, Foster in combination with Adams and Tsai teach the system as described per claim 11 (See rejection of claim 11 above).

Foster in combination with Adams and Tsai does not teach wherein the buffer monitor provides a buffer pointer to the processor to control the movement of writes from the processor to the buffer.

However, Okbay teaches wherein the buffer controller includes a write pointer to the buffer (Okbay; Paragraph [0038] Lines 1 – 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Foster in combination with Adams and Tsai to include the buffer pointer because doing so allows for the CPU

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to know where the next available memory location for writing and reading is (Okbay; Paragraph [0038] Lines 1 – 5).

6. Claims 9 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,948,081 (hereinafter Foster) in view of US Patent Application Publication No. 2005/0273528 (hereinafter Adams) further in view of US Patent Application Publication No. 2003/0079059 (hereinafter Tsai) and further in view of US Patent Application Publication No. 2002/0065948 (hereinafter Morris).

As per claims 9 and 26, Foster in combination with Adams and Tsai teach the method and system as described per claims 1 and 11 (See rejection of claims 1 and 11 above).

Foster in combination with Adams and Tsai does not teach providing a timeout signal indicating when a transaction is not cleared from the buffer within a predetermined amount of time and clearing the buffer and external bus transaction in response thereto.

However, Morris teaches flushing a buffer in response to a timeout condition (Morris; Paragraph [0008] Lines 8 – 12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Foster in combination with Adams and Tsai to include the buffer flushing after timeout because doing so allows for resources to be restored back to the system.

***Allowable Subject Matter***

7. Claims 6 – 7, 19 – 21, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form ***including all of the limitations of the base claim and any intervening claims.***

8. Claim 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to ***include all of the limitations of the base claim and any intervening claims.***

Claims 6 – 7 and 19 – 21 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record fails to teach or suggest alone or in combination that providing control over a rate of a number of writes provided to the buffer further comprises ***providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto***, as required by dependent claims 6 and 19, ***in combination with the other recited claim limitations*** (emphasis added). Support for this limitation can be found in the originally filed specification at page 13 lines 16 – 20. Prior art of reference, US Patent No. 5,948,081 (hereinafter Foster), teaches asserting an almost full signal, but is silent on providing a vector to a register indicating the almost full condition. US Patent Application Publication No. 2005/0273528 (hereinafter Adams) teaches forcing an error condition, but does not teach providing a register with a vector representing the error condition. US Patent Application Publication No. 2003/0079059

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(hereinafter Tsai) teaches slowing a data rate in response to a threshold being hit, but does not teach slowing in response to scanning a register and determining when a number of writes in the buffer is static.

Claim 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112 2<sup>nd</sup> Paragraph and put into independent form including all of the limitations of the base claim and any intervening claims because the prior art of record fails to teach or suggest alone or in combination ***determining whether an external interface is hung based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer and clearing the buffer and external bus transactions when the external interface is hung***, as required by dependent claim 10, ***in combination with the other recited claim limitations*** (emphasis added). Support for this limitation can be found in the originally filed specification at page 14 line 18 – page 15 line 3. The prior art of reference teaches the limitations as described per claim 1 (see rejection of claim 1 above), but fails to teach detecting a static buffer pointer representing a lack of movement of writes in the buffer.

Claim 23 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record fails to teach or suggest alone or in combination ***wherein the error conditions comprise anticipated error conditions based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer***, as required by

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dependent claim 23, *in combination with the other recited claim limitations* (emphasis added). Support for this limitation can be found in the originally filed specification at page 14 line 12 – page 15 line 3. The prior art of reference teaches the limitations as described per claim 11 (see rejection of claim 11 above), but fails to teach detecting a static buffer pointer representing a lack of movement of writes in the buffer.

### **Conclusion**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.



DONALD SPARKS  
SUPERVISORY PATENT EXAMINER

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin  
Patent Examiner  
Art Unit 21811